UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 17-cv-05671-BLF

ORDER DENYING VLSI'S MOTION FOR RELIEF FROM NONDISPOSITIVE PRETRIAL ORDER OF MAGISTRATE JUDGE

[Re: ECF No. 652]

Plaintiff VLSI Technology, LLC ("VLSI") filed a Motion for Relief from Magistrate Judge Nathanael M. Cousins' Nondispositive Pretrial Order (ECF No. 604 ("Order")), which struck two of VLSI damages expert Dr. Ryan Sullivan's theories on the grounds that VLSI did not disclose them in its damages contentions. ECF No. 652 ("Mot."). VLSI asks this Court to reverse Judge Cousins' Order on the grounds that it "overlooked that VLSI . . . disclosed and explained both of Dr. Sullivan's theories, but used slightly different labels to do so." Mot. at 1.

VLSI's motion is DENIED for the reasons described below.

I. BACKGROUND

VLSI accuses Intel Corporation's ("Intel") Turbo Boost Max Technology 3.0 ("TBMT") feature of infringing U.S. Patent No. 8,566,836 (the "'836 Patent"). On May 16, 2023, Intel moved to strike, *inter alia*, two of VLSI damages expert Dr. Ryan Sullivan's '836 Patent damages theories – Value Per Unit ("VPU") and Net Present Value ("NPV") – on the grounds that VLSI failed to disclose either theory in its Fifth Supplemental Damages Contentions (ECF No. 476-1, ("FSDC")). ECF No. 473. Judge Cousins ordered additional briefing on the motion, which the parties provided. ECF Nos. 502, 507. On August 30, 2023, Judge Cousins issued an order granting Intel's motion to strike the VPU and NPV damages theories. Order at 8. Pursuant to

Federal Rule of Civil Procedure 72 and Civil Local Rule 72-2, VLSI filed an objection to the Order (Mot.) and, pursuant to the Court's briefing schedule (ECF No. 655), Intel responded. ECF No. 699 ("Opp.").

II. LEGAL STANDARD

Pretrial orders issued by a Magistrate Judge may be reversed only if they contain "clear error." *Grimes v. City & Cnty. of San Francisco*, 951 F.2d 236, 241 (9th Cir. 1991).

III. DISCUSSION

A. Judge Cousins' Findings

VLSI argues that the following formula disclosed in its FSDC provides the basis for both its NPV and VPU damages theories. Mot. at 1–2 (citing FSDC at 99). VLSI asserted in its briefing to Judge Cousins that "the NPV and VPU values" are the economic value parameter used in the formula, and that both "derive from two Intel documents – 89699DOC01565734 and 93000DOC03579403." Order at 7 (citing ECF No. 502 at 8).

- **Reasonable Royalty = Economic Value of Accused Feature × Accused Revenues (or Accused Units) × Cost Apportionment Factor x Contribution Apportionment Factor**

Judge Cousins first found that the FSDC properly disclosed that "experts may rely on 'Intel data and testimony.'" Order at 6 (quoting FSDC at 82). Judge Cousins then addressed the two documents put forth by VLSI to determine if they disclosed the VPU and NPV theories.

Judge Cousins determined that the first document, 89699DOC01565734, was not properly disclosed. He noted that the document was cited three times in the FSDC. *Id.* He found that the first two references appear in VLSI's description of the technical benefits of the '836 Patent. *Id.* (citing FSDC at 49, 57). He then found that the third reference appears in a separate section describing the costs associated with implementing the accused features, as opposed to the value the technology brings to Intel. *Id.*; *compare* FSDC at 101 (discussing costs associated with the accused technology) *with* ECF No. 476-3 ("Sullivan Report") ¶ 408 ("Intel anticipated TBMT 3.0 to generate $345 million in net present value ("NPV") for desktop ("DT") and mobile ("MB") products"). Due to the disparate placement of such references, Judge Cousins concluded that it

would be unreasonable for Intel to infer that VLSI would implement the computations to demonstrate economic value. *Id.*

The Court finds no clear error in Judge Cousins' finding regarding document 89699DOC01565734. The three citations to 89699DOC01565734 in the FSDC pertain to technical specifications or costs and have nothing to do with VPU or NPV damages, much less economic value of any kind. *See* FSDC at 49 ("Intel also ran a test showing [redacted]") (citing 89699DOC01565734); *id.* at 57 ("VLSI also expects that its experts will analyze the recently-produced data illustrating Intel's testing of the accused features.") (citing 89699DOC01565734); *id.* at 102 ("Another document indicates that [redacted]") (citing 89699DOC01565734).

Judge Cousins found that the second document, 93000DOC03579403, "suffers from similar infirmities." Order at 7. He specifically noted that, "[f]or example, VLSI points to one citation among over ten pages of string citations" (*id.* (citing FSDC at 85)) and concluded that "[s]uch vague and imprecise citations to internal documents and analyses does not give Intel notice of VLSI's theory and promotes the 'type of inferential guesswork . . . [the] damages contentions are intended to avoid.'" *Id.* (quoting *Looksmart Grp., Inc. v. Microsoft Corp.*, 386 F. Supp. 3d 1222, 1234 (N.D. Cal. 2019).

The Court disagrees with Judge Cousins' finding that the second document, 93000DOC03579403, was not properly disclosed. But as discussed below, this disagreement does not change the outcome. While, as Judge Cousins notes, one citation to 93000DOC03579403 is in a nearly 14-page string cite, the document is cited eight other times throughout the FSDC. *See* FSDC at 49, 83, 84, 98, 102, 167. Some of these citations correspond to technical information, but three citations specifically refer to economic assessments that related to economic value. *See* FSDC at 49 ("Intel noted that [redacted], and that '[redacted]'") (quoting 93000DOC03579403); *id.* at 83 ("For example, one Intel document indicates [redacted]

[redacted]") (quoting 93000DOC03579403–04); *id.* at 84 ("***Intel's internal documents*** relating to marketing and pricing strategy demonstrate [redacted], ***including Turbo Boost Max Technology 3.0*** (which is accused of infringing the '836 Patent), [redacted].") (citing, *inter alia*, 93000DOC03579403) (emphasis added). The Court concludes that these three citations constitute a sufficient disclosure that TBMT could be linked to damages theories including, for example, an [redacted]

Judge Cousins found that because these two documents were not properly cited, "VLSI does not disclose either the NPV or VPU as theories of recovery in its Contentions." Order at 7.

Judge Cousins also addressed Intel's argument that VLSI did not properly disclose underlying data for Dr. Sullivan's VPU and NPV theories. Intel argued in its discovery letter to Judge Cousins that "Sullivan relies on twelve Intel documents ([Sullivan Report] ¶¶ 408-09, 414, 417, 428, 429, 430) for the inputs to his calculation, but VLSI did not disclose using a single one in its damages calculation." ECF No. 473. Instead, Intel argued, "[VLSI] buried four of them in string cites among hundreds of other documents and did not cite eight of them at all." *Id.* VLSI responded in its supplemental briefing to Judge Cousins that it properly "disclose[d] eight of twelve Intel documents Dr. Sullivan supposedly relies on for his damages opinion. Two of these eight documents are duplicates of documents cited in the contentions, and Dr. Sullivan uses them merely to provide background for his analysis." ECF No. 502 at 8. Judge Cousins agreed with Intel, and found that VLSI's "scattershot references ***to Intel data*** or documents do not support Sullivan's application of the NPV or VPU calculations." Order at 6 (emphasis added).

The Court reviews Judge Cousins' Order for clear error.

B. Value Per Unit (VPU) Data Was Not Properly Disclosed

VLSI argues that Dr. Sullivan's VPU theory is "based on Intel's anticipated 'sell-up' benefit of TBMT." Mot. at 3. Specifically, Dr. Sullivan opines in his report that adding TMBT would "result in an [redacted]" in a "per-unit reasonable royalty calculation." *Id.* (citing Sullivan Report

¶¶ 428–29). Intel takes issue first with VLSI's use of the terms "sell-up" and "upsell" and second with the source of the [redacted] numbers. Opp. at 3–4.

First, VLSI argues that the terms "sell-up" and "upsell" fairly disclose a VPU damages theory. VLSI argues that it "repeatedly disclosed that TBMT enables Intel to charge a price premium for products that have TBMT, and thereby provides 'sell-up' and 'up sell' benefits." Mot. at 3. Specifically, VLSI claims it disclosed that "Intel's documentation estimates that [TBMT] '[redacted].'" *Id.* (quoting FSDC at 84).

Intel responds that VLSI never argued to Judge Cousins that "it referred to Dr. Sullivan's methodologies as a 'sell up'" and has thus waived it. Opp. at 1. Intel also argues that "VLSI's contentions refer to a 'sell up' just one single time, in a section describing alleged ***technical benefits*** of TBMT." *Id.* at 4 (citing FSDC at 50:3–12) (emphasis in original).

The Court agrees with VLSI. First, the Court finds no functional distinction in the meaning of the terms "upsell," "sell up," increase in "average sale price" ("ASP"), and increase in "value per unit." These terms all stand for a simple damages principle: an increase in the sale price of a unit. The Court finds that VLSI did not waive this argument because it addressed disclosure of increases in ASP in its supplemental briefing to Judge Cousins. ECF No. 502 at 8 (citing FSDC at 82). The Court also disagrees with Intel's claim that "upsell" and "sell-up" are only referred to in a technical context. The FSDC clearly disclosed the [redacted] in an economic context. *See* FSDC at 83 ("For example, one Intel document indicates an [redacted]") (citing 93000DOC03579403–04); *id.* at 84.

Second, VLSI disagrees with Judge Cousins' determination that it "provided only 'scattershot references' to underlying documents, which 'do not support Sullivan's application of the NPV or VPU calculations.'" Mot. at 1 (quoting Order at 6). VLSI cites to its disclosure of the [redacted]upsell, and "several additional documents" cited in the FSDC, then claims that the documents "discuss these same benefits, each of which were also discussed in Dr. Sullivan's report, or are substantively identical to documents discussed in Dr. Sullivan's report." *Id.* at 4.

Intel responds that VLSI did not "disclose it would use the [redacted] sales numbers"

cited in paragraphs 428–430 of the Sullivan Report and that it therefore "had no way to know from VLSI's contentions that Dr. Sullivan would get to a damages number using an [redacted] sales increase from Intel's documents or a VPU calculation." Opp. at 3

The Court agrees with Intel. VLSI explains that Dr. Sullivan's VPU theory is based on data that TBMT would "result in [redacted]." Mot. at 3. But VLSI does not address disclosure of those [redacted] in the FSDC. Even if VLSI properly disclosed a VPU theory in the context of a [redacted], Dr. Sullivan does not utilize the [redacted] figure in his damages opinions. VLSI failed to disclose underlying data for a VPU damages calculation based on the [redacted] sales increases which were clearly identified in documents in existence at the time of filing damages contentions. Since VLSI does not squarely address this disclosure, the Court finds no clear error in Judge Cousins' determination.

Having found no clear error in Judge Cousins' determination that VLSI did not properly disclose the data underlying Dr. Sullivan's VPU theory in the FSDC, the Court DENIES VLSI's Motion for Relief as to the VPU theory.

C. Net Present Value (NPV) Theory and Data Were Not Properly Disclosed

VLSI argues that the FSDC discloses the documents Dr. Sullivan used for his NPV theory. Mot. at 5 (citing Sullivan Report at ¶¶ 413–419). First, VLSI asserts that an FSDC citation to an email describing TBMT as a "[redacted]" disclosed the NPV theory, but that Judge Cousins "appears to have overlooked" the email. Mot. at 5 (citing 93000DOC02370250). Second, VLSI argues that it "cited at least four separate versions of the specific NPV documents in VLSI's discussions of the '836 Patent's technical value and benefits." *Id.*

Intel responds to both arguments. First, Intel argues that Dr. Sullivan does not purport to use the [redacted] figure from 93000DOC02370250 for any part of or input to his NPV computation. Opp. at 5 (citing Sullivan Report at ¶¶ 413–427). Intel adds that VLSI's contentions cite the document only in a section addressing purported technical benefits, which is not sufficient to disclose a NPV theory. *Id.* (citing FSDC at 50). Second, Intel argues that "VLSI did not disclose in its contentions that any of [the NPV documents have] anything to do with NPV or a

damages computation" but instead "cited the documents only as relating to issues such as performance benefits, testing, or costs associated with the accused feature." *Id.* (citing FSDC at 49:8–16, 56:20–58:9, 101:26–102:6, 128:16–139:19).

The Court finds no clear error in Judge Cousins' exclusion of the NPV theory. First, Judge Cousins hardly "overlooked" the email; VLSI's briefing never directed Judge Cousins to the document. VLSI claimed instead that the two documents Judge Cousins did review (89699DOC01565734 and 93000DOC03579403) were the "two specific Intel documents that VLSI cited throughout its contentions" that disclose VPU and NPV. ECF No. 502 at 8. Despite this, VLSI did not cite either the quote, the dollar figure, or even the page number from the FSDC that contained the citation (FSDC at 50) in its original briefing to Judge Cousins. A court cannot be expected to find a single sentence and citation buried in a 226-page document without direction from the parties' briefing.

Even if VLSI had properly made this argument to Judge Cousins, the quote does not properly disclose the NPV theory. VLSI's only basis for the NPV theory is the single quote from a once-cited document claiming that TBMT represents a "[redacted]" for Intel. FSDC at 50 (quoting 93000DOC02370250). A single email claiming a financial opportunity with no other context hardly puts an opposing party on notice of a NPV damages theory.

VLSI's second argument that other documents disclose the NPV theory also fails. The four new documents put forth by VLSI (Mot. at 5) are contained in a string cite in the FSDC describing "the recently-produced data illustrating Intel's testing of the accused features." FSDC at 57 (the fifth document listed is 89699DOC01565734, which Judge Cousins and this Court agree did not properly disclose economic value related to damages theories). A label about recently produced testing data in no way discloses any kind of damages theory, much less one related to NPV. Therefore, the Court finds that Judge Cousins committed no clear error in striking the NPV damages theory.

Having found no clear error in Judge Cousins' determination that VLSI did not properly disclose the data and theory underlying Dr. Sullivan's NPV theory in the FSDC, the Court DENIES VLSI's Motion for Relief as to the NPV theory.

IV. ORDER

For the foregoing reasons, IT IS HEREBY ORDERED that Plaintiff VLSI's Motion for Relief from Magistrate Judge Nathanael M. Cousins' Nondispositive Pretrial Order (ECF No. 652) is DENIED.

Dated: October 11, 2023

BETH LABSON FREEMAN
United States District Judge